PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Moon et al.

Serial No.: 09/874,631

Filed: June 5, 2001

For: FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES

Confirmation No.: 5108

Examiner: S. Clark

Group Art Unit: 2815

Attorney Docket No.: 2269-4368US
(99-0959.00/US)

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Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of U.S. patents are not being submitted pursuant to M.P.E.P. 609 III A(2). Copies of foreign patent documents and non-patent literature are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an

admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
US - 3,239,496	03/1966	Jursich
US - 4,074,342	02/1978	Honn et al.
US - 4,818,728	04/1989	Rai et al.
US - 5,148,265	09/1992	Khandros
US - 5,346,861	09/1994	Khandros
US - 5,404,044	04/1995	Booth et al.
US - 5,468,681	11/1995	Pasch
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US - 5,683,942	11/1997	Kata
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US - 5,777,391	07/1998	Nakamura
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US - 5,905,303	05/1999	Kata
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US - 6,133,637	10/2000	Hikita et al.
US - 6,177,723	01/2001	Eng et al.
US - 6,217,343	04/2001	Okuno
US - 6,222,265	04/2001	Akram et al.
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Foreign Patent Documents

Document No.	Publication Date	Patentee
EP 0684644	11/1995	Kata et al.
EP 1009027	06/2000	Okuno
KR 2001054744	07/2001	Choi et al. (English Abstract)

Other Documents

AL-SARAWI et al., "A review of 3-D packaging technology," Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol 21, Issue 1, Feb. 1998, pp. 2-14.

ANDROS et al., "TBGA Package Technology," Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol. 17, Issue 4, Nov. 1994, pp. 564-568.

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FERRANDO et al., "Industrial approach of a flip-chip method using the stud-bumps with a non-conductive paste," Adhesive Joining and Coating Technology in Electronics Manufacturing, 2000. Proceedings. 4th International Conference on, 18-21, June 2000, pp. 205-211.

GALLAGHER et al., "A Fully Additive, Polymeric Process for the Fabrication and Assembly of Substrate and Component Level Packaging," The First IEEE International Symposium on Polymeric Electronics Packaging, 26-30, Oct. 1997, pp. 56-63.

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HATANAKA, H., "Packaging processes using flip chip bonder and future directions of technology development," Electronics Packaging Technology Conference, 2002. 4th, 10-12, Dec. 2002, pp. 434-439.

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LEE et al., "Enhancement of Moisture Sensitivity Performance of a FBGA," Proceedings of International Symposium on Electronic Materials & Packaging, 2000, pp. 470-475.

LI et al., "Stencil Printing Process Development for Flip Chip Interconnect," IEEE Transactions Part C: Electronics Packaging Manufacturing, Vol. 23, Issue 3, (July 2000), pp. 165-170.

LYONS et al., "A New Approach to Using Anisotropically Conductive Adhesives for Flip-Chip Assembly, Part A, " *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* Vol. 19, Issue 1, March 1996, pp. 5-11.

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TEUTSCH et al, "Wafer Level CSP using Low Cost Electroless Redistribution Layer," *Electronic Components and Technology Conference*, 2000. 2000 Proceedings. 50th, 21-24 May 2000, pp. Pages: 107-113.

"The 2003 International Technology Roadmap for Semiconductor: Assembly and Packaging."

TSUI et al., "Pad redistribution technology for flip chip applications," *Electronic Components and Technology Conference*, 1998. 48th IEEE, 25-28 May 1998, pp. 1098-1102.

XIAO et al., "Reliability study and failure analysis of fine pitch solder-bumped flip chip on low-cost flexible substrate without using stiffener," IEEE, 2002. Proceedings 52nd, 28-31 May 2002, pp. 112-118.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed concurrently with an RCE in the above-identified application, and therefore no additional fee is due.

Respectfully submitted,

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Date: September 24, 2004
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 4

Complete if Known	
Application Number	09/874,631
Filing Date	June 5, 2001
First Named Inventor	Moon et al.
Group Art Unit	2815
Examiner Name	S. Clark
Attorney Docket Number	2269-4368US (99-0959.00/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-3,239,496	03/1966	Jursich	
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
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